Phase-Locked Loop Techniques—A Survey

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(Invited Paper)

***Abstract*— Phase-locked loop (PLL) is a technique which has contributed significantly toward the technology advancement in communication and motor servo control systems in the past 30 years. Inventions in PLL schemes combining with novel integrated circuit (IC) technology have made PLL devices important system components. The development of better modular PLL IC's is continuing. As a result, it is expected that it will contribute to improvement in performance and reliability for future communication systems. It will also contribute to the development of higher accuracy and higher relibility servo control systems, such as those involved in machine tools. This paper serves as an introduction for this PLL Special Section. It provides a concise review of the basic PLL principles applicable to communication and servo control systems, gives the configurations of PLL applications, and reports a number of popular PLL chips.**

I. Introduction

AN EARLY description of phase-locked loop (PLL) appeared in the papers by Appleton [1] in 1923 and de Bellescize [2] in 1932. The advent of PLL has contributed to coherent communication systems without the Doppler shift effect. In the late 1970's, the theoretical description of PLL was well established [13], [16], [19], but PLL did not achieve widespread use until much later because of the difficulty in realization. With the rapid development of integrated circuits (IC's) in the 1970's, the applications of PLL were widely used in modern communication systems. Since then, the PLL has made much progress and has turned its earlier professional use in high-precision apparatuses into its current use in consumers' electronic products. It has enabled modern electronic systems to improve performance and reliability, especially in common electronic appliances used daily.

In the 1970's, researchers in the control field first paid attention to the realization of PLL for a synchronous motor speed control system [31]. Since then, phase-locked servo systems (PLS's) were rapidly developed for ac and dc motors' servomechanisms using analog PLL IC's [41]–[49]. Over the past 10 years, the rapidly developed high-performance digital IC's and microprocessors have strongly motivated the implementation of PLS using digital technology. This has led to the development of new types of controllers with added PLS features for achieving an easy-use and easy-control nature for ac and dc servo drives [45], [50]–[53], [56], [57].

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II. Basic Concept of PLL

A PLL is a device which causes one signal to track another one. It keeps an output signal synchronizing with a reference input signal in frequency as well as in phase. More precisely, the PLL is simply a servo system, which controls the phase of its output signal in such a way that the phase error between output phase and reference phase reduces to a minimum. The functional block diagram of a PLL is shown in Fig. 1, which consists of a phase detector (PD), a loop filter (LF), and a voltage-controlled oscillator (VCO). Let x_i and x_o be, respectively, the input and the VCO signals, which can be expressed as [13], [16], [19]

$$x_i(t) = A\cos(\omega_i t + \theta_i) \tag{1}$$

$$x_o(t) = B\cos(\omega_o t + \varphi_o). \tag{2}$$

ω_i and ω_o are angular frequencies of the input signal and the VCO; θ_i and φ_o are their phase constants. The PD is a signal multiplier. If the loop is initially unlocked and the phase detector has a sinusoidal characteristic, the significant output signal $v_e(t)$ at the PD is given by

$$v_e(t) = K_d\{\cos[(\omega_i - \omega_o)t + \theta_i - \varphi_o] + \cos[(\omega_i + \omega_o)t + \theta_i + \varphi_o]\} \tag{3}$$

where K_d is the gain of the PD. The higher frequency component with frequency $\omega_i + \omega_o$ is eliminated by LF, a low-pass filter. Therefore the output of the LF is

$$v_c(t) = K_d\cos[(\omega_i - \omega_o)t + \theta_i - \varphi_o]. \tag{4}$$

After a period of time sufficiently long for transient, the VCO output signal x_o becomes synchronous with the input signal x_i. The signal x_o can then be expressed as

$$x_o(t) = B\sin(\omega_i t + \phi_o). \tag{5}$$

Comparing (2) and (5) shows that the phase φ_o in (2) is a linear function of time given by

$$\varphi_o = (\omega_i - \omega_o)t + \phi_o \tag{6}$$

and the LF output signal $v_c(t)$ in (4) becomes a dc signal given by

$$v_c(t) = K_d\cos(\theta_i - \phi_o). \tag{7}$$

The VCO is a frequency-modulated oscillator, whose instantaneous angular frequency ω_{inst} is a linear function of the

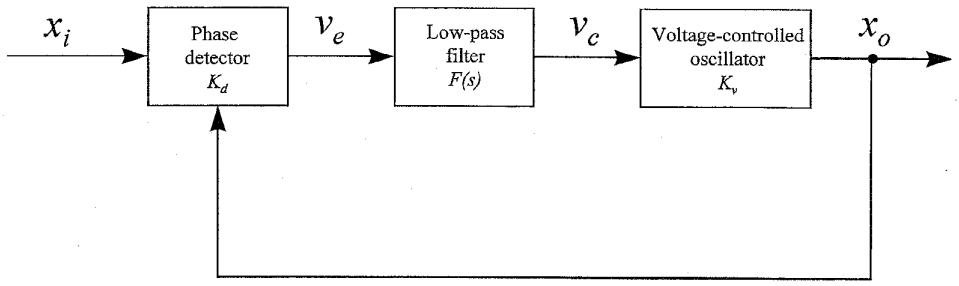

Fig. 1. Basic topology of the PLL.

controlled signal $v_c(t)$, around the central angular frequency ω_o, i.e.,

$$\omega_{\text{inst}} = \frac{d}{dt}(\omega_o t + \varphi_o) = \omega_o + K_v V_c(t) \tag{8}$$

and

$$\frac{d\varphi_o}{dt} = K_v v_c(t) \tag{9}$$

where K_v is the VCO sensitivity. From (6), (7), and (9)

$$\omega_i - \omega_o = K_d K_v \cos(\theta_i - \phi_o) \tag{10}$$

giving

$$\phi_o = \theta_i - \cos^{-1}\frac{\omega_i - \omega_o}{K_d K_v}. \tag{11}$$

Substituting (11) into (7) yields

$$v_c = \frac{\omega_i - \omega_o}{K_v}. \tag{12}$$

Equation (12) clearly shows that it is the dc signal v_c that changes the VCO frequency from its central value ω_o to the input signal angular frequency ω_i, i.e.,

$$\omega_{\text{inst}} = \omega_o + K_v v_c = \omega_i. \tag{13}$$

If the angular frequency difference $\omega_i - \omega_o$ is much lower than the product $K_d K_v$, (11) gives $\theta_i - \phi_o \approx \cos^{-1} 0 = \pi/2$, indicating that the VCO signal is in phase quadrature with the input signal when the loop is in lock. Strictly speaking, the phase quadrature corresponds to $\omega_i = \omega_o$. Thus it is convenient to let

$$\theta_o = \phi_o + \frac{\pi}{2}. \tag{14}$$

Then (7) becomes

$$v_c = K_d \sin(\theta_i - \theta_o). \tag{15}$$

The difference $\theta_i - \theta_o$ is the phase error between the two signals, which is null when the initial frequency offset is null. When the difference $\theta_i - \theta_o$ is sufficiently small, the following approximation is used:

$$v_c \approx K_d(\theta_i - \theta_o). \tag{16}$$

In view of (14), (11) can be expressed as

$$\phi_o = \theta_i - \cos^{-1}\frac{\omega_i - \omega_o}{K_d K_v}. \tag{17}$$

The product $K = K_d K_v$ is referred to as the loop gain. When the difference $|\omega_i - \omega_o|$ exceeds the loop gain K in a sinusoidal-characteristic PD, a proper θ_o for lock can no longer exit as evidenced by (17). Under this condition, synchronization can no longer maintain and the loop falls out of lock.

III. Phase Detector

There are two types of PD's, namely, the sinusoidal PD's and the square signal PD's. A sinusoidal PD inherently has phase detection interval $(-\pi/2, +\pi/2)$. It operates as a multiplier, which is a zero memory device. The square signal PD's, also called sequential PD's, are implemented by sequential logic circuits. Sequential PD's contain memory of past events, which can generate PD characteristics that are difficult or impossible to obtain with multiplier circuits. They are usually built up from digital circuits and operate with binary rectangular input waveforms. Accordingly, they are often called digital phase detectors. The characteristics of the square signal PD's are of the linear type over the phase detection interval $(-\pi/2, +\pi/2)$ for triangular PD, $(-\pi, +\pi)$ for sawtooth PD, and $(-2\pi, +2\pi)$ for sequential phase/frequency detector (PFD) [3], [4], [6], [9], [12], [15]. Their characteristics are depicted in Fig. 2 [16]. All curves of Fig. 2 are shown with the same slope at phase error $\theta_e = \theta_i - \theta_o = 0$, which means that the different PD's all have the same factor K_d. Increasing PD phase detection interval provides a larger tracking range, larger lock limit, than those obtainable from a sinusoidal PD.

IV. Voltage-Controlled Oscillator

The voltage-controlled oscillators (VCO's) used in the PLL basically are not different from those employed for other applications, such as modulation and automatic frequency control. The main requirements for the VCO are 1) phase stability, 2) large frequency deviation, 3) high modulation sensitivity K_v, 4) linearity of frequency versus control voltage, and 5) capability for accepting wide-band modulation. The phase stability requirement is in direct opposition to all other four requirements. Four types of VCO commonly used are given in the order of decreasing stability, namely, voltage-controlled crystal oscillators (VCXO's), resonator oscillators, RC multivibrators, and YIG-tuned oscillators [13], [16]. The phase stability can be enhanced by a number of ways: 1)

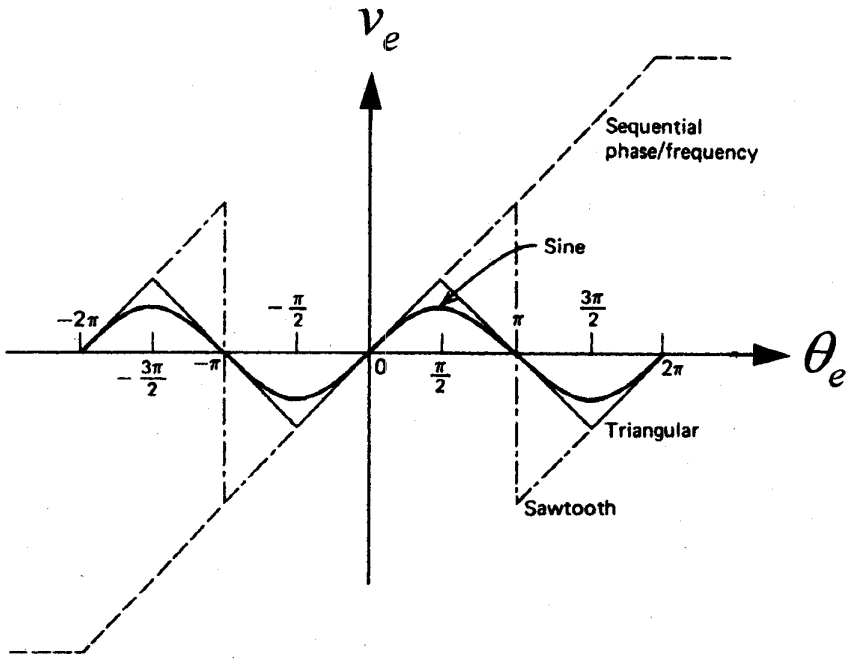

Fig. 2. Characteristics of the phase detector (taken from [4]).

using high Q crystal and circuit, 2) maintaining low noise in the amplifier portion, 3) stabilizing temperature, and 4) keeping mechanical stability. Most of the phase jitter of an oscillator arises from noise in the associated amplifier. If a wider frequency range is required, an LC oscillator must be used. In this application, the standard Hartley, Colpitts, and Clapp circuits make their appearance. The tuning is accomplished by means of a varactor, junction capacitance of a diode. At microwave frequencies, YIG-tuned Gunn oscillators have become popular. Tuning of the YIG-tuned oscillator is accomplished by altering a magnetic field.

V. Loop Filter and Other Subsystems

The LF in PLL is a low-pass filter. It is used to suppress the noise and high-frequency signal components from the PD and provide a dc-controlled signal for the VCO. We assume that the loop is in lock, that the PD is linear, and the LF output voltage is proportional to phase error. The phase error voltage v_e is filtered by the loop filter. The servo scheme of the PLL in linear locking state is shown in Fig. 3, where $F(s)$ is the loop transfer function. According to servo terminology, the type of the loop is determined by the number of perfect integrators within the loop. Any PLL is at least a type-one loop because of the perfect integrator inherent in the VCO. If the loop filter contains one perfect integrator, then the loop is type two. A second-order PLL with a high-gain active filter can be approximated as a type-two loop, whereas a PLL with a passive filter is type one. The widely used passive and active filters for the PLL are shown in Fig. 4. The closed-loop transfer function of the PLL for the passive filter is given by

$$H'(s) = \frac{K_v K_d(s\tau_2 + 1)/\tau_1}{s^2 + s(1 + K_v K_d \tau_2/\tau_1) + K_v K_d/\tau_1}. \tag{18}$$

For the active filter

$$H''(s) = \frac{K_v K_d(s\tau_2 + 1)/\tau_1}{s^2 + s(K_v K_d \tau_2/\tau_1) + K_v K_d/\tau_1}. \tag{19}$$

For convenience in description, (18) and (19) can be rewritten into the forms

$$H'(s) = \frac{s(2\zeta\omega_n - \omega_n^2/K_v K_d) + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{20}$$

and

$$H''(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{21}$$

in which ω_n is the natural frequency of the loop and ζ is the damping ratio. The relevant parameters for passive filter are

$$\omega_n = \left(\frac{K_v K_d}{\tau_1}\right)^{1/2}$$

$$\zeta = \frac{1}{2}\left(\frac{K_v K_d}{\tau_1}\right)^{1/2}\left(\tau_2 + \frac{1}{K_v K_d}\right)$$

$$\tau_1 = (R_1 + R_2)C$$

and

$$\tau_2 = R_2 C \tag{22}$$

and for active filter are

$$\omega_n = \left(\frac{K_v K_d}{\tau_1}\right)^{1/2}$$

$$\zeta = \frac{\tau_2}{2}\left(\frac{K_v K_d}{\tau_1}\right)^{1/2} = \frac{\tau_2 \omega_n}{2}$$

$$\tau_1 = R_1 C$$

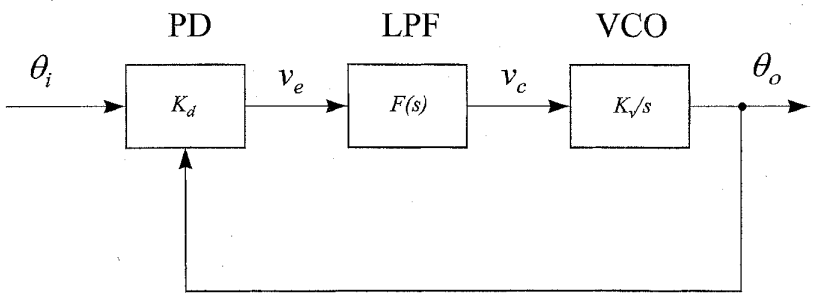

Fig. 3. Linear model of the phase-locked loop.

and

$$\tau_2 = R_2 C. \tag{23}$$

The two transfer functions are nearly the same if $1/K_v K_d \ll \tau_2$ in the passive filter. The open-loop transfer function of any PLL has the form

$$G(s) = \frac{K_v K_d F(s)}{s}. \tag{24}$$

The closed-loop transfer function can be given by

$$H(s) = \frac{G(s)}{1 + G(s)}. \tag{25}$$

Define the dc gain of the loop as

$$K_D = K_v K_d F(0). \tag{26}$$

A large value of K_D is usually required for achieving a good performance of the loop [16]. Define the hold-in range of a loop as $\Delta\omega_H = K_D$. If the input frequency is sufficiently close to the VCO frequency, a PLL locks up with just a phase transient; there is no cycle slipping prior to lock. The frequency range over which the loop acquires phase to lock without slips is called the lock-in range of the PLL. In a first-order loop, the lock-in range is equal to the hold-in range, but for the second- or higher order loops, the lock-in range is always less than the hold-in range. Besides, there is a frequency interval, smaller than the hold-in interval and larger than the lock-in interval, over which the loop will acquire lock after slipping cycles for a while. This interval is called the pull-in range. Their relations are indicated in Fig. 5. To ensure stable tracking, it is common practice to build loop filters with equal numbers of poles and zeros. At high frequencies the loop is indistinguishable from a first-order loop with gain $K = K_d K_v F(\infty)$. As a fair approximation, we can say that the higher order loop has the same lock-in range as the equivalent-gain first-order loop. The lock-in limit of a first-order loop is equal to the loop gain. We argue here that a higher order loop has nearly the same lock limit. The lock-in range $\Delta\omega_L$ can be approximately estimated as

$$\Delta\omega_L \approx \pm K_d K_v F(\infty). \tag{27}$$

Acquisition of frequency in PLL is more difficult and slower, and requires more design attention than phase acquisition. The self-acquisition of frequency is known as frequency pull-in, or simply pull-in, and the self-acquisition of phase is known as phase lock-in, or lock-in.

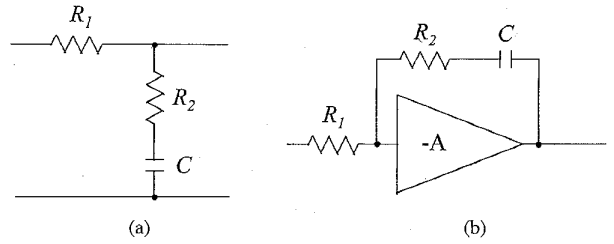

Fig. 4. (a) Passive filter. (b) Active filter.

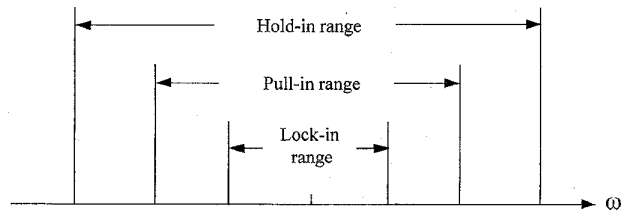

Fig. 5. Ranges of the dynamic limits of a PLL.

VI. Configurations of PLL Applications

Integrated phase-locked loops developed since the 1970's are versatile systems, which are suitable for use in a variety of frequency-selective demodulation, signal conditioning, or frequency-synthesis applications. PLL techniques in communication are well developed and widely used for FM, AM, video, signal processing, telecommunication systems, etc. PLL's are widely applied in versatile systems as reference signal sources or oscillators. Besides, PLL is frequently realized as a signal modulator or synthesizer due to its inherent configuration. Fig. 6 is a phase modulator formed by the phase-locked loop. The modulating signal $m(t)$ combining with the phase error from the PD modulates the PLL to achieve a phase modulation and indirect frequency modulation. A typical phase-locked indirect synthesizer is shown in Fig. 7, in which N is the division factor. The output frequency is synthesized by $N \cdot f_{\text{ref}}$.

The use of PLL with analog PLL IC (NE565 developed by Signetics) for a synchronous motor and for a dc motor began in the 1970's [32]–[38], [45]. A PLS system is a frequency feedback control configuration that continuously maintains the motor speed or the motor position by tracking the phase and frequency of the incoming reference signal that corresponds to the input command, such as speed or position. Basically,

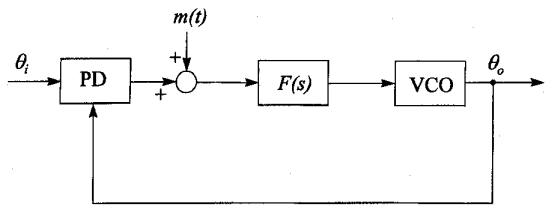

Fig. 6. Phase modulator by PLL.

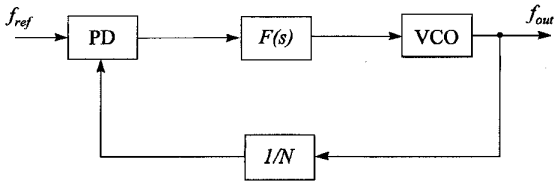

Fig. 7. Synthesizer PLL.

the PLS configuration is a combination of a phase detector, a loop filter, and a servo motor, as shown in Fig. 8, in which the servo motor acts as the VCO of the basic PLL. The use of PLL for a synchronous motor speed control began in the 1970's. Volpe [31] indicated that a synchronous motor can be viewed as a PLL if the motion of its rotor and stator fields are analogous to the VCO signal and to the reference input signal, respectively, of a PLL. The motor's speed will vary synchronously with the reference input. This leads to the result that a synchronous motor's rotor position responding to the stator's electrical phase input is equivalent to a highly underdamped second-order PLL. In order to regulate speed, Volpe presented a two-loop control for a PLL synchronous motor. Due to the rapid progress in digital IC's, a phase-error detection range from $-\pi$ to $+\pi$ was obtained by using a sawtooth comparator in the 1970's [16], when the optical encoder for converting the motor rotation to digital pulses was also available. In order to extend the lock range of PLL, a PFD, capable of phase-error detection ranging from -2π to $+2\pi$, was achieved by using a sequential logic technique [34]. A PLS consisting of a PFD, an LF, and a motor with an optical encoder has been realized. Using the PFD's wide detection range, a speed regulation of up to 0.002% in PLS was achieved [34]. Tal proposed the analysis of PLS by a sampled-data control technique [40] to estimate the low speed limitation, the lock range, and the design problems.

In 1980, Gardner [18] unified the description of a charge-pump controller, which includes current-pump and voltage-pump modes. This has become an accepted argument for the behavior of an analog controller for PLL and PLS after all. Gardner stated that the charge pump can be modeled as a three-position electronic switch, which is controlled by the three states of the PFD, namely, up, down, and neutral. In 1985, Margaris and Petridis [50] proposed a voltage-pump model, formed by a positive feedback from the filter capacitor voltage, which is presented to provide a nearly zero steady-state speed error in the PLS for increasing the speed accuracy.

In 1987, Hsieh *et al.* [51] proposed an adaptive digital pump controller (ADPC) to achieve a phase-locked speed servo system (DPPLS). The ADPC can completely replace traditional charge-pump controllers and has a quantized linear tracking range from -2π to $+2\pi$. No pulse-like voltage jumps will superimpose onto the pumped voltage and the speed response of the DPPLS has no disturbance during the locking process. Furthermore, the line densities of the optical encoder used in the PLS can be reduced, resulting in more stability and cost improvement. In 1989, Hsieh [53] first proposed a frequency-pumped controller (FPC) for a frequency-locked position servo control system (FLPS). The utilization of the FPC is to achieve a position control by the frequency-locked technique. In order to reduce the speed acquisition time for the large speed difference command, a microprocessor-based slope-varied digital-pumped controller (μP-SVDPC) was presented [52]. Through the slope-varied process, the proposed μP-based digital-pump phase-locked servo system (μP-DPPLS) can achieve nearly the same speed acquisition time for small or large speed difference commands.

The PLL applied for induction motors was first published during 1975–1981 [27], [31]. A phase-controlled oscillator [(PCO), as a controller] suitable for phase-locked stepping motor servo systems was realized in 1992 [56]. It can provide an accurate and stable pulse train to achieve a phase-locked stepping servomechanism (PLSS). The latest stepping position servo system based on the frequency-locked technique (SP-SCS) was proposed for high-performance incremental position control in 1995 [57]. The position acquisition time for the presented SPSCS system has improved by approximately 67–79% compared to the corresponding traditional position control system.

VII. Analog, Digital, and Hybrid PLL's

Due to rapid progress in analog and digital IC's in the 1970's, the integrated PLL has been developed for filtering, frequency synthesis, motor-speed control, frequency modulation, demodulation, signal detection, and a variety of other applications. The configuration of PLL's can be either analog or digital, but most of them are hybrids composed of both analog and digital components. The first analog PLL IC's, NE565 and CD4046, were developed by Signetics and RCA in the 1970's. They are integrated on a chip including a sinusoidal PD, an LF, and a VCO. The phase detector is a multiplier, whose phase-lock range is from $-\pi/2$ to $+\pi/2$. In order to extend the lock-in range of PLL, the Motorola digital PFD MC4044 capable of phase-detection range from -2π to $+2\pi$ was proposed in 1972 [34]. A hybrid PLL realized by combining discrete analog and digital components was then achieved. Hereafter, the versatile PLL's components for improving the locking performance are developed in succession. Nowadays, it is a future-exploited trend to integrate the PD, prescaler, programmable counter, and VCO on a chip IC to form a PLL module device. The difficulty for realizing chip PLL is how to constitute a high-frequency VCO on a single chip IC, which operates at a frequency above 2.5 GHz [20]. The type of PLL used in the realization system is determined according to the application [17]–[21].

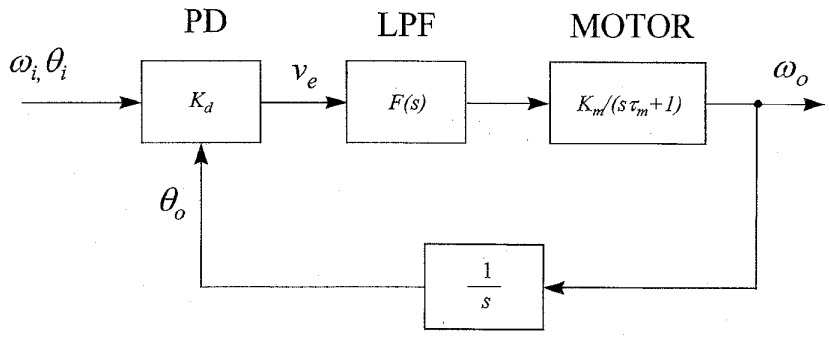

Fig. 8. Linear model of the phase-locked servo loop.

VIII. Popular PLL Integrated Circuits (IC's)

A wide variety of IC's for PLL are available from semiconductor manufacturers. The techniques widely used to implement the PLL are transistor–transistor logic (TTL), complementary metal-oxide-semiconductor (CMOS), and emitter-coupled logic (ECL). Nowadays, fully integrated PLL on a single chip can operate at frequencies up to 35 MHz, such as Exar XR-215 PLL. Other higher frequency PLL's are easily achieved by combining sub-PLL IC's (including only PD, prescaler, and programmable counter) and discrete higher-frequency VCO's. It is an important trend to realize fully integrated higher frequency PLL formed by constituting a high-frequency VCO into a modulus device in the near future. Nowadays, Motorola and Plessey are developing versatile PLL IC's operating at frequencies above 2.5 GHz. The Motorola MC 12210 is a 2.5-GHz bipolar monolithic series-input phase-locked loop synthesizer with phase-swallow function. It is designed for the high-frequency local oscillator of an RF transceiver in handheld communication applications. This PLL IC can operate at a minimum supply voltage of 2.7 V for input frequencies up to 2.5 GHz with a typical current drain of 9.5 mA. A dual modulus prescaler is integrated to provide either a 32/33 or 64/65 divide ratio [21]. Besides, new Motorola VCO's MC12147 and MC12149 with operating frequency up to 1.1 GHz were introduced in 1995 [23]. The GEC Plessey SP5070 and SP5655 are, respectively, 2.4-GHz and a 2.7-GHz single modulus frequency synthesizers for use in satellite TV receivers, high IF cable tuning systems, and C-band with frequency doubling mixer. Both two PLL synthesizers operate at a low power consumption (5 V and 30 mA). The SP5655 capable of standard I2C BUS control format contains two addressable current-limited outputs and four addressable bidirectional open collector ports, one of which is a three-bit ADC. The information on these ports can be read via the I^2C BUS. The device has one fixed I^2C BUS address and three programmable addresses, programmed by applying a specific input voltage to one of the current-limited outputs. This enables two or more synthesizers to be used in a system [22].

IX. Conclusions

This paper gives a concise review of the PLL technique, which is applicable to communication and servo control systems. The status of the PLL technology and its applications have been discussed. A summary of the PLL technology and its development trends are also included. It is pointed out that the development of better PLL technology and the associated modular IC's is continuing. The PLL-based servo control systems has become important and popular in the development of mechatronics.

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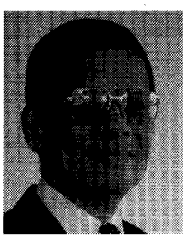

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