COURSE GUIDE
Academic year 2019-2020

Dean,
Professor Daniela Tărniceriu, PhD

1. Date despre program

1.1 Higher education institution	"Gheorghe Asachi" Technical University of Iaşi
1.2 Faculty / Department	Electronics, Telecommunications and Information Technology
1.3 Department	Telecommunications and Information Technologies
1.4 Field	Electronic Engineering, Telecommunications and Information Technology
1.5 Study level	Bachelor's Degree Studies
1.6 Study program / Qualification	Telecommunications Technologies and Systems

2. Course info

2.1 Course name	**Computer-Aided Design of Analog and Digital Systems**					Code	EDID311T
2.2 Lecturer	Dănuţ Burdia, Associate professor, PhD						
2.3 Applications	Dănuţ Burdia, Associate professor, PhD Felix Diaconu, Lecturer, PhD						
2.4 Year of study	**3**	2.5 Semester	**6**	2.6 Assessement	**Exam**	2.7 Category	**DS**

3. Estimated total time (hours per semester for teaching activities)

3.1 Number of hours per week	**5**	3.2 lecture	**2**	3.3b lab	**2**	3.3c project	**1**
3.4 Total number of hours in curricula	**70**	3.5 lecture	**28**	3.6b lab	**28**	3.6c project	**14**

Time distribution	hours
Textbook, course support, references and course notes study	14
Library, electronic platforms and on site documentation	4
Seminar/laboratory preparation, homework, reports, portfolios and essays	14
Tutoriing	7
Assessment	4
Other activities – advice, consultation	4

3.7 Total individual study hours	**50**
3.9 Total hours per semester	**120**
3. 10 Number of credit points	**5**

4. Prerequisites (where applicable)

4.1 curriculum	Computer-Aided Analysis of Electronic Circuits
4.2 competences	Basic algebra (linear equation systems), matrix operations, differential equations, Boolean algebra, logic gates and circuits, basic programming languages, computer skills

5. Infrastructure (where applicable)

5.1. de desfasurare a cursului	Course hall or lecture theater with capacity of minimum 50 students. Equipements: blackboard or whiteboard with accesorises, desktop computer or laptop, video projector (beam), projection screen, crete or white board marker.

5.2. de desfasurare a laboratorului	- Laboratory room with min. 9 workstations with internet access. Software tools: OrCad PSpice, ModelSim, Xilinx ISE Design Suite internet browser, text editor, Adobe Reader. - Laboratory work must be fully carried out, the results being noted at each session. Students will be presented to the laboratory with a brief summary of the laboratory's essay. Homework must be presented at deadline. Delays in delivery have to be justified. Presentation at exam is conditioned by attending and graduating the applications with colloquium, homeworks and project.

6. Specific skills acquired

Competence profesionale	• Know the terminology used in computer-aided design of analog and digital circuits. • Demonstrate the appropriate use of nonlinear resistive network analysis methods based on hybrid representation • Understand the importance of knowing the methods and algorithms underlying the time domain analysis of linear and nonlinear dynamic networks • Demonstrate the ability to correctly apply the principles of designing logic gates. • Demonstrate the appropriate modeling capability of digital circuits using hardware description languages • Identify and choose the optimal methods for implementing test circuits • Develop skills for the correct use of modeling and simulation tools for analog and digital circuits
Competence transversale	- To make efficient use of information resources and communication and training resources in the field of computer-aided design of analogue and digital circuits - Demonstrate preoccupation for professional development through the training of critical thinking skills and to improve their training and education throughout the course of their work. - Develop team work skills and become familiar with an environment dedicated to modeling and simulating digital circuits with the help of hardware description languages

7. Course target (as resulting from **6. Specific skils acquired** table)

7.1 Obiectivul general al disciplinei	Developing theoretical and practical skills in the field of nonlinear and dynamic nonlinear resistive network analysis, as well as in the field of modeling and simulation of digital circuits using hardware description languages
7.2 Obiectivele specifice	- - Understand and apply the principles of formulating a linear resistive multiport and determining the hybrid representation - - Demonstrate acquiring knowledge of methods of analysis of nonlinear resistive networks based on hybrid representation - - Understand and apply methods for formulating state equations for linear dynamic networks - - Demonstrate the knowledge of the state equation solving algorithms for time domain analysis of nonlinear dynamic networks - - Understand the basic concepts of hardware description languages - - Understand and apply the principles of modeling digital circuits using hardware description languages - - Learn the syntax of VHDL - - To demonstrate the principles and techniques of construction of test circuits using hardware description languages - - Demonstrate acquiring skills for the correct use of simulation tools for analog electronic circuits and graphical representation of the results. - - Demonstrate learning skills of simulation and synthesis tools of digital circuits - modeled in hardware description languages.

8. Contents

8. 1 Lectures	**Teaching methods**	**Notes**
Part I: Hardware description language - VHDL		
Introduction to digital circuit design using VHDL	-lecturing	1 lecture
Basic terminology of VHDL (entity, architecture, configuration,		2 lectures

package)	-beam using	
Basics of VHDL (objects, data types, operators)	-explanations	1 lecture
Structural modeling in VHDL	-debate	1 lecture
Data-flow modeling in VHDL	- discussions	1 lecture
Behavioral modeling in VHDL		1 lecture
Advanced topics of VHDL (functions, procedures)		1 lecture
Part 2: Advanced topics of analog circuit simulation		
Algorithms for formulating of hybrid equations for linear resistive n-ports		2 lectures
Nonlinear resistive network analysis by hybrid method		1 lecture
Formulating the state equations for linear dynamic networks		1 lecture
Numerical solving the state equations for nonlinear dynamic networks		1 lecture
Multistep integration algorithms for nonlinear dynamic network analysis		1 lecture

References

1. Chua L.O. and P.M. Lin, Computer Aided Analysis of Electronic Circuits, Prentice Hall, 1975.
2. D. Burdia, Computer-Aided Analysis of Electronic Circuits (Romanian), Tehnopres, Iaşi, 2009 (ch. 6-10)
3. D. Burdia, G.S. Popescu Computer-Aided Design of Electronic Circuits:. SPICE and VHDL (Romanian), Part I: SPICE, Matrixrom, 1999.
4. D. Burdia,
5. Vlach, J. and K. Singhal, Computer Methods for Circuit Analysis and Design, New York, van Nostrand Reinhold, 1983
6. Ruehli A.E., Circuit Analysis, Simulation and Design, Advances in CAD for VLSI, vol. 3, North-Holland, 1987
7. Jenkins D.G. and R.C. Welland, Software Engineering for Electronic Systems, IEE Computing Series 18, 1990.
8. J. Bhasker, A VHDL Primer, Prentice Hall, 1995
9. S. Sjoholm, L. Lindh, VHDL for Designers, Prentice Hall, 1997
10. R.S. Cooper, The Designer's Guide to Analog&Mixed-Signal Modeling Illustrated with VHDL-AMS and MAST, Avant!Corporation, 2001

10.D.L. Perry, VHDL: Programming by Example, McGraw-Hill, 2002

11. P.P.Chu, RTL Hardware Design Using VHDL, Willey-Interscience, 2006.

8. 2 Laboratory	Teaching method	Notes
1. Safety workimg rules. Overview of SPICE circuit netlist editing.	Practical demonstration Exercises	
2. Overview of circuit analysis using SPICE. Macromodels of electronic devices (operational amplifier)		
3. Principles of CMOS Logic gates design		
4. Simulation and performance evaluation of CMOS logic gates		
5. Using PSpice AD for Mixed and Digital Circuits simulation		
6. Basic principle of VHDL. Project compilation and simulation.		
7. VHDL model simulation using testbenches		
8. Data-flow and structural modeling using VHDL		
9. Structural modeling using generate statement. Behavioral modeling using VHDL		
10. VHDL description of Finite State Machines		
11. Advanced VHDL : functions, procedures and packages		
12. VHDL modeling and simulation of a multiplier algorithm		

13. FPGA synthesis using Xilinx ISE tool		
8.3 Project	Teaching methods	Notes
The project consists of two parts. The first part consists in the design of a bistable circuit at the transistor level and the simulation of their dynamic parameters. The second part consists of VHDL modeling and testing of a digital circuit (numerator, decoder, stopwatch, circuits based on finite state machines, s.a)	Demonstration, exercise, error analysis	

Bibliografie

- D. Burdia, Computer Aided Design of Analog and Digital Systems, Laboratory Guidance
- http:\\www.etti.tuiasi.ro/pac
- *** The Design Center, Circuit Analysis Reference Manual, MicroSim Corp., 1994
- www.pspice.com - manuale de utilizare Pspice A/D 9.2, analiza circuitelor
- http://www.vhdl-online.de/~vhdl - VHDL tutorial, aplicatii
- www.eda.org - Electronic Design Automation

9. Corroborating the contents discipline expectations epistemic community representatives, professional associations and employers representative for the field program

In determining the content of discipline and teaching methods / examination discipline holders have consulted with counterparts from both the Romanian academic community and from abroad. Also, it has taken into account the opinion and expectations of key industry players in Romania, with which the faculty has collaboration. Course objectives are consistent with the curriculum, passing on information and skills necessary for forming future specialists in electronics and telecommunications.

11. Assessment

Activity type	10.1 Assessment criteria	10.2 Assessment Methods	10.3 Percentage of final grade
10.4 Lectures	• Theoretical knowledge acquired (quantity, correctness, accuracy)	Intermediate tests:	10 %
		Homeworks:	%
		Final exam: writing exam	50 % (minim 5)
10.5b Laboratory	Knowledge of equipment, how to use specific tools; assessment tools or achievements, processing and interpretation of results	- written questionnaire - oral answer - laboratory notebook (experimental works, essays) - practical demonstration	15 % (minim 5)
10.5c Project	Quality of the project done, accuracy of project documentation, justification of solutions chosen	• Evaluation, presentation and / or support the project • Critical evaluation of a project	25% (minim 5)
10.6 Minimum performance standard			
Knowing the fundamentals of theory, problem solving, behavioral or structural VHDL modeling of a simple circuit			

Completion date:
13.09.2019

Course organizer signature,
Dănuţ Burdia, Associate Professor

Teaching assistant signature,
Dănuţ Burdia, Associate Professor

Felix Diaconu, Lecturer

16. SEP. 2019

Date of advice in department

Head of Department signature

Luminiţa Scripcariu, Associate Professor, PhD